Zeen Fang

Microelectronics / Modelling / AI for EDA

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EDUCATION

Central South University | B.Eng. in Microelectronics Science and Engineering | September 2023 - June 2027 (expected)

Weighted average: 89.43/100. CET-6: 576. Selected coursework: semiconductor device physics, analog and digital electronics, computer principles and architecture, EDA, and large-scale integrated circuit design.

RESEARCH DIRECTION

Seeking Fall 2027 PhD opportunities in AI for EDA, chip design space exploration and hardware verification. My current foundation is device and circuit modelling, parameterised simulation, controlled comparisons and research validation.

CODEX-ENABLED RESEARCH WORKFLOWS

I have used Codex to connect workflows in TCAD, Cadence Virtuoso and PSpice: model and experiment setup, parameter sweeps, data extraction, result checks, figures and manuscript preparation. Each environment retains its own solver. I define the research question and comparison conditions and review the original outputs.

RESEARCH & ENGINEERING

Memristor read-write interface | First-author published study

Derived operating constraints from the VTEAM state equation and evaluated a time-separated read-write interface through behavioural modelling, analytical comparisons and simulation. Published in Electronics; this is a pre-silicon modelling study.

Second-order memristor SPICE model | Ongoing research

Developing a PSpice model with retained conductance and relaxing history states. Matched-state and history-off comparisons connect internal-state attribution to circuit behaviour. Manuscript in preparation; simulation only.

Top-gate In2O3 TFT scaling | Third-author collaboration

Contributed validation, data curation, and manuscript review and editing to a numerical study of short-channel effects and simulated DC/RF behaviour, published in Micromachines.

LDO design and verification | Competition team project

Contributed selected schematic-analysis, PVT/PSRR/stability, physical-verification and post-layout tasks in a SMIC 180 nm, 1.8 V LDO team project. Regional hardware involved a separate semi-discrete LDO. No tapeout or silicon measurement.

PUBLICATIONS

Fang, Z., Zhu, M., Xu, H., & Zhang, L. (2026). Memristor-Based Read-Write Interface Design for Neural Networks: A Comparative Study of Linear-Drift and VTEAM Models. *Electronics, 15*(11), 2333. DOI

Xu, H., Zhu, M., Fang, Z., & Zhang, L. (2026). Numerical Investigation of Short-Channel Effects and RF Performance in Top-Gate In2O3 Thin-Film Transistors. *Micromachines, 17*(5), 567. DOI

SELECTED HONOURS

2026: National Final Second Prize, IC Innovation and Entrepreneurship Competition, Zengyi Huichuang Track (team). 2026: Mathematical Contest in Modeling, Honorable Mention (team). 2024: First Prize, Hunan Division, Chinese Mathematics Competition for College Students.